

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



538216



(43) International Publication Date
1 July 2004 (01.07.2004)

PCT

(10) International Publication Number
WO 2004/055904 A1

(51) International Patent Classification⁷: H01L 29/78,
29/423, 21/336

(21) International Application Number:
PCT/IB2003/006015

(22) International Filing Date: 8 December 2003 (08.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0229217.5 14 December 2002 (14.12.2002) GB

(71) Applicant (for all designated States except US): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): SCHMITZ, Jurriaan [NL/NL]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). HUETING, Raymond, J., E. [NL/NL]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). HIJZEN, Erwin, A. [NL/BE]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). MONTREE, Andreas, H. [NL/NL]; c/o Philips Intellectual Property & Standards,

Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). IN T ZANDT, Michael, A., A. [NL/NL]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). KOOPS, Gerrit, E., J. [NL/BE]; c/o Philips Intellectual property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HAS (GB).

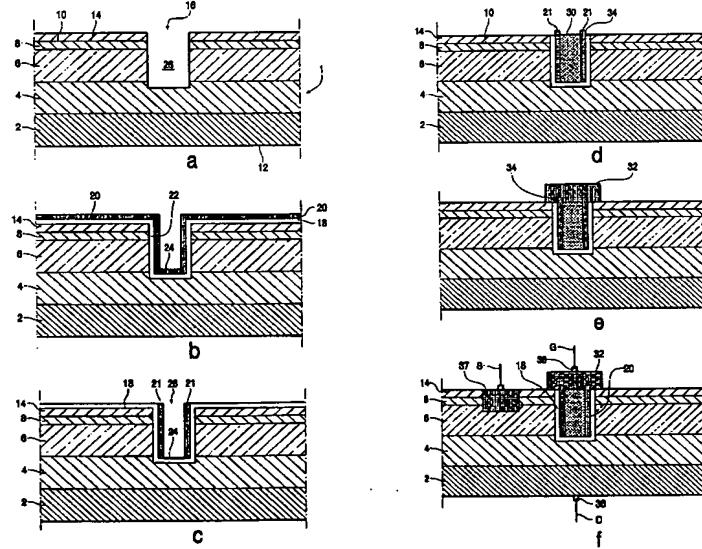
(74) Agent: SHARROCK, Daniel, J.; Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: VERTICAL INSULATED GATE TRANSISTOR AND MANUFACTURING METHOD



WO 2004/055904 A1

(57) Abstract: A vertical insulated gate transistor is manufactured by providing a trench (26) extending through a source layer (8) and a channel layer (6) towards a drain layer (2). A spacer etch is used to form gate portions (20) along the trench side walls, a dielectric material (30) is filled into the trench between the sidewalls gate portions (20), and a gate electrical connection layer (30) is formed at the top of the trench electrically connecting the gate portions (20) across the trench.